SWARNANDHRA
COLLEGE OF ENGINEERING & TECHNOLOGY
(AUTONOMOUS)
Accredited by National Board of Accreditation, AICTE, New Delhi, Accredited by NAAC with "A" Grade – 3.32 CGPA, Recognized under 2(f) & 12(B) of UGC Act 1956, Approved by AICTE, New Delhi, Permanent Affiliation to JNTUK, Kakinada
Seetharampuram, W.G.DT., Narsapur-534280, (Andhra Pradesh)

DEPARTMENT OF INFORMATION TECHNOLOGY
TEACHING PLAN

Course Code	Course Title	Semester	Branch	Contact Periods /Week	Academic Year	Date of commencement of Semester
20IT3T02	COMPUTER ORGANIZATION	III	IT	5	2021-2022	25-10-2021

COURSE OUTCOMES	
1	Explain knowledge on structure of computers and computer arithmetic.
2	Analyze Micro operations such as Arithmetic micro operations, Shift micro operations and Logic micro operations.
3	Define the appropriate addressing modes and instructions for writing programs.
4	Demonstrate the Peripheral devices for efficient operation of system.
5	Describe the basic knowledge on parallel and vector processing.

UNIT	Out Comes / Bloom's Level	Topics No.	Topics/ Activity	Text Book/ Reference	Contact Hour	Delivery Method
I	CO – 1	1.1	Introduction	T2	1	Chalk & Board; Power point presentations; Assignment; Test
		1.2	Basics of computer	T2	1	
		1.3	Von Neumann Architecture	T2	1	
		1.4	Generation of Computer	T2	1	
		1.5	Types of Computer	T2	1	
		1.6	Functional unit	T2	1	
		1.7	Basic Operational Concepts	T2	1	
		1.8	Bus Structures	T2	1	
		1.9	Arithmetic Addition	T1	1	
		1.10	Arithmetic Subtraction	T1	1	
		1.11	Multiplication algorithms	T1	1	
		1.12	Division Algorithms	T1	1	
Content beyond syllabus		1.13	Floating point arithmetic operations	T1	1	
				Total	13	
II		2.1	Register Transfer language	T1	1	Chalk & Board
		2.2	Register Transfer Bus	T1	1	
		2.3	Memory transfers	T1	1	
		2.4	Arithmetic Micro operations	T1	1	

	CO – 2	2.5	logic micro operations	T1	1	Power point presentations Assignment Test
		2.6	shift micro operations	T1	1	
		2.7	Arithmetic logic shift unit	T1	1	
		2.8	Instruction codes	T1	1	
		2.9	Computer Registers	T1	1	
		2.10	Computer Instructions	T1	1	
		2.11	Timing and control	T1	1	
		2.12	Instruction Cycle	T1	1	
		2.13	Memory – Reference	T1	1	
		2.14	Input – Output and Interrupt Instructions	T1	1	
		2.15	Design of basic computer	T1	1	
		2.16	Design of Accumulator logic	T1	1	
Content beyond syllabus		2.17	Hardware description languages	T1,T3	1	
				Total	17	
III	CO – 3	3.1	General Register Organization	T1	1	Chalk & Board Power point presentations Assignment Test
		3.2	STACK organization	T1	1	
		3.3	Instruction formats	T1	1	
		3.4	Addressing modes	T1	1	
		3.5	Data Transfer and manipulation	T1	1	
		3.6	Program control	T1	1	
		3.7	Reduced Instruction Set Computer	T1	1	
		3.8	Control Memory	T1	1	
		3.9	Address sequencing	T1	1	
		3.10	micro program example	T1	1	
		3.11	design of control unit	T1	1	
Content beyond syllabus		3.12	Problems on Micro programmed control	T1,T3	T1	
				Total	12	
IV	CO – 4	4.1	Peripheral Devices	T1	1	Chalk & Board Power point presentations Assignment
		4.2	Input-Output Interface	T1	1	
		4.3	Asynchronous data transfer	T1	1	
		4.4	Modes of Transfer	T1	1	
		4.5	Priority Interrupts	T1	1	
		4.6	Direct memory Access	T1	1	
		4.7	Memory Hierarchy	T1	1	
		4.8	Main Memory	T1	1	

		4.9	Auxiliary memory	T1	1	Test
		4.10	Associative Memory	T1	1	
		4.11	Cache Memory	T1	1	
		4.12	Virtual Memory	T1	1	
				Total	12	
V	CO – 5	5.1	Parallel Processing	T1, R1	1	Chalk & Board
		5.2	Pipelining	T1, R1	1	
		5.3	Arithmetic Pipeline	T1, R1	1	
		5.4	Instruction Pipeline	T1, R1	1	Power point presentations
		5.5	RISC Pipeline	T1, R1	1	
		5.6	Vector Processing	T1, R1	1	
		5.7	Three segment instruction pipeline	T1, R1	1	Assignment
		5.8	Array Processors	T1, R1	1	Test
Content beyond syllabus		5.9	Super scalar processors	T1, R1	1	
				Total	9	
			CUMULATIVE PROPOSED PERIODS		63	

Text Books:

S.No.	AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION
1	M. Moris Mano, Computer System Organization, 3rd Edition, Pearson / PHI, 2017.
2	Carl Hamacher, Zvonks Vranesic, SafeaZaky, Computer Organization, 5th Edition, McGraw Hill, 2016.
3	John L. Hennessy and David A.Patterson, Computer Organization, a quantitative approach, Fifth Edition, 2017.

Reference Books:

S.No.	AUTHORS, BOOK TITLE, EDITION, PUBLISHER, YEAR OF PUBLICATION
1	William Stallings, Computer Organization and Architecture, Ninth Edition, Pearson / PHI, 2012.
2	Andrew s. Tanenbaum, Structured Computer Organization, 6th Edition, PHI/ Pearson, 2016.

Web Details:

1	**https://www.javatpoint.com/computer-organization-and-architecture-tutorial**
2	**https://www.geeksforgeeks.org/computer-organization-and-architecture-tutorials/**

		Name	Signature with Date
i.	Faculty	Mr. Ch Rama Krishna Raju	25/10/21
ii.	Module Coordinator	Mr. Ch Rama Krishna Raju	25/10/21
iii.	Programme Coordinator	Dr. RVVSV Prasad	25/10/21

Principal